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10/529,310	03/25/2005	Uzi Vishkin	MR2833-39	8642

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EXAMINER	
BAHTA, KIDEST	
ART UNIT	PAPER NUMBER
2123	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/529,310	VISHKIN, UZI	
	Examiner	Art Unit	
	KIDEST BAHTA	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *36-58* is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/21/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-5, 8, 10, 12-15,17-18, 21-25, 28, 33 and 34 are rejected under 35 U.S.C. 102(e) as being anticipated by Cochran et al. (US 6,848,841).

Regarding claims 1 and 25, Cochran discloses a computer structure, including processing elements and memory elements, the computer structure comprising: a plurality of individual modules (column 1, lines 5-15, i.e., many electronic or computerized devices and equipment, regardless of size, are a managed interconnection of many different subsystems. Such electronic computing equipment (e.g. disk arrays, computers, routers, switches) utilize a shared copper conductor crossbar switch or bus backplane for interconnecting the subsystem components (e.g. processors, cache, shared memory disk controllers, host interface cards, each of said modules having said processing elements for processing data and at least one of said memory elements for storing data therein (Fig. 1 and 2, element 202 and 201); an optical interconnect structure coupled to each of said plurality of modules for optically transporting

data (Fig. 1 and 2); and a plurality of optical communication channels, each coupled between respective two of said plurality of chips to form an all-to-all interconnection there between to transport data in optical form thereof between said respective chips (Fig. 2, column 3, lines 27-52).

Regarding claims 2-5, 8, 10, 12-15, 17-18, 21-24, 28, 33 and 34, Cochran discloses,

2. The computer structure of claim 1, wherein said memory elements of said plurality of the modules form a shared memory (element 201).

3. The computer structure of claim 2, wherein said memory elements on each of said plurality of modules comprises the highest level of the memory hierarchy (Fig. 1, element 107 and 109).

4. The computer structure of claim 1, wherein said processing elements include parallel processing elements (Fig. 2, elements 202 and 204).

5. The computer structure of claim 1, wherein said optical interconnect structure includes a plurality of optical communication channels coupled to respective said modules to form an all-to-all interconnection therebetween (Fig. 2).

8. The computer structure of claim 5, wherein said waveguide channels form a double plane waveguide and wherein at least one of said plurality of optical communication channels bends over at least another of said plurality of optical communication channels (fig. 2).

10. The computer structure of claim 5, further comprising a plurality of optoelectronic components (column 10, lines 30-44), each of said plurality of optoelectronic components being coupled between an end of at least one respective optical communication channel and a respective one of said plurality of modules (Fig. 2).

12. The computer structure of claim 10, wherein each of said plurality of optoelectronic components includes a photodetector coupled by an input thereof to a receiving end of said at least one respective optical communication channel to receive an optical signal therefrom, said photodetector generating an electrical signal corresponding to said optical signal, said electrical signal being coupled to an input port of said respective module.

13. The computer structure of claim 10, wherein said plurality of optoelectronic components reside on said optical interconnect structure (Fig. 2).

14. The computer structure of claim 10, further comprising storage elements associated with receiving and sending ends of said optical communication

channels of said optical interconnect structure to temporarily store therein data (column 3, lines 8-25).

15. The computer structure of claim 5, wherein receiving ends of a portion of said plurality of optical communication channels are coupled to the same destination one of said plurality of modules, further comprising means at said destination module for conflict-free access of data to said destination module (Fig. 3, column 3, lines 38-52)

17. The computer structure of claim 1, wherein the transport of the data in said optical interconnect structure is based on decentralized routing scheme (Fig. 8 and 9).

18. The computer structure of claim 1, wherein said optical interconnect structure is pipelined (Fig. 7).

21. The computer structure of claim 5, wherein one optical communication channel bends over another optical communication channel, thus avoiding crossing thereof in a single plane.

22. The computer structure of claim 5, wherein not more than two optical communication channels cross at the same crossing point (column 3, lines 8-26).

23. The computer structure of claim 22, wherein a distance between two crossing points is below a predetermined value (Fig. 3).

24. The computer structure of claim 22, wherein beyond said crossing point, a distance between two of said plurality of optical communication channels is below a predetermined spacing (column 4, lines 57-66).

28. The interconnection fabric of claim 25, wherein said shared memory comprises a first-level cache and wherein said processing elements form the processing elements of a parallel computer system (fig. 2).

33. The interconnection fabric of claim 26, wherein not more than two optical waveguides of said plurality thereof cross at the same crossing point (column 4, lines 17-36).

34. The interconnection fabric of claim 33, wherein a distance between two crossing points is above a predetermined value ((column 4, lines 57-66).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which

said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 6-7, 9, 26-27, 29 and 32, 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cochran et al. (US 6,848,841) in view of Blalock et al. (US 7,006,746).

Regarding claims 6-7, 9, 26-27, 29 and 32, 35, Cochran discloses the limitation of 1, 5, 25, as stated above, but fails to disclose the limitationes of 6-7, 9, 26-27, 29 and 32, 35. However, Blalock discloses the limitations of claims 6-7, 9, 26-27, 29 and 32, 35 as follw:

6. The computer structure of claim 5, wherein said optical communication channels include waveguide channels formed on a substrate (column 7, lines 4-18).

7. The computer structure of claim 6, wherein said waveguide channels extend and intersect in a single plane (Abstract).

9. The computer structure of claim 5, wherein said optical communication channels of said interconnect structure include optical fibers.

26. The interconnection fabric of claim 25, wherein said plurality of optical communication channels is formed as a plurality of waveguides fabricated on a substrate (Fig. 1 and 2).

27. The interconnection fabric of claim 26, wherein at least two of said plurality of said optical waveguides extend and intercross at a crossing point in a single plane on said substrate (Fig. 11, column 9, lines 23-48).

29. The interconnection fabric of claim 26, wherein at least one of said plurality of optical waveguide is bended (column10, lines 26-38).

32. The interconnection fabric of claim 26, wherein at least one of said plurality of optical waveguides bends over at least another optical waveguide (column10, lines 26-38)..

35. The interconnection fabric of claim 33, wherein beyond said crossing point, a distance between said at least two optical waveguide is above a predetermined spacing (Fig. 11, 14).

It would have been obvious to a person of ordinary skill in the art at the time of invention was made to modify the teachings of Cochran with the teachings of Blalock since the effective index between the waveguide and grating can be matched, thereby allowing the synchronicity requirements to be met for larger bandwidth devices.

Allowable Subject Matter

5. Claims 36-58 allowed.

6. Claims 11, 16, 19, 20, 30-31, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed Kidest Bahta whose telephone number is 571-272-3737. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application information Retrieval IPAIRI system. Status information for published applications may be obtained from either Private PMR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAG system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-fee).

/Kidest Bahta/

Primary Examiner, Art Unit 2123